

CLAIMS

I claim:

- 5 1. A first-in-first-out (FIFO) module comprising:
 - a memory bank having a plurality of individually addressable memory locations;
 - a write pointer that is connected to the memory bank for addressing a first memory location of the plurality of memory locations to write data on an
 - 10 input data bus into the first memory location;
 - a read pointer that is connected to the memory bank for addressing a second memory location of the plurality of memory locations to read data in the second memory location onto an output data bus; and
 - 15 at least one additional pointer that is connected to the memory bank for addressing a third memory location of the plurality of memory locations to read data stored in the third memory location.
- 20 2. A FIFO module according to Claim 1, further comprising a detector that is connected to the memory bank for receiving the data read from the third memory location and comparing the read data with a predetermined datum to determine if there is match.
- 25 3. A FIFO module according to Claim 1, wherein the at least one additional pointer comprises a look-back pointer that is coupled to the write pointer for addressing a third memory location that trails the first memory location.
4. A FIFO module according to Claim 3, wherein the third memory location is at least one memory location behind the first memory location.

5. A FIFO module according to Claim 3, wherein the write pointer and the look-back pointer are driven by a common clock signal and wherein the third memory location is the first memory location at least one clock cycle after the first memory location is written to.

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6. A FIFO module according to Claim 5, wherein an address of the third memory location is readable from the FIFO module.

7. A FIFO module according to Claim 1, wherein the at least one additional pointer comprises a look-ahead pointer that is coupled to the read pointer to address a third memory location that leads the second memory location.

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8. A FIFO module according to Claim 7, wherein the third memory location is at least one memory location ahead of the second memory location.

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9. A deskew circuit comprising:

at least two FIFO modules, each of the at least two FIFO modules comprising:

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a memory bank having a plurality of individually addressable memory locations;

a write pointer that is connected to the memory bank, the write pointer storing a write address that is increasable for addressing the memory locations to write data therein;

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a look-back pointer that is coupled to the write pointer for addressing a first memory location that trails a second memory location addressable by the write pointer; and

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a detector that is connected to the memory bank for comparing data in the third memory location with an alignment datum, the detector asserting a datum-found signal when the datum in the third memory location matches the alignment datum; and

a skew compensation unit that is connected to the at least two FIFO modules for receiving addresses of respective third memory locations of the at least two FIFO modules when the respective datum-found signals are asserted, and for thereby determining a skew using the addresses and generating a control signal for controlling the write pointer of one of the at least two FIFO modules to compensate for the skew.

10. A deskew circuit according to Claim 9, wherein the skew compensation unit comprises a skew compensation unit for receiving addresses of respective third memory locations that are latched by the respective datum-found signals.

11. A deskew circuit according to Claim 10, wherein the skew compensation unit comprises a skew compensation unit for receiving latched addresses of respective third memory locations that are synchronized to a clock that drives the skew compensation unit.

12. A deskew circuit according to Claim 9, wherein the control signal for controlling the write pointer of one of the at least two FIFO modules comprises a control signal that inhibits increase of the write address in the write pointer for a period corresponding to the skew.

13. A rate matching circuit comprising:

at least one FIFO module comprising:

a memory bank having a plurality of individually addressable memory locations;

a write pointer that is connected to the memory bank for addressing the memory locations to write data therein;

a read pointer that is connected to the memory bank for addressing memory locations to read data therefrom; wherein the write pointer and read pointer are driven by separate clock signals;

a look-ahead pointer that is coupled to the read pointer for addressing a first memory location that leads a second memory location addressable by the read pointer;

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a flag circuit that generates a trigger signal when a difference of addresses in the write pointer and the read pointer exceeds a predetermined threshold; and

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a detector that is connected to the memory bank for comparing data in the first memory location with a skip datum, the detector asserting a datum-found signal when the data in the first memory location matches the skip datum; and

a rate matcher connected to the at least one FIFO module for receiving the trigger signal and the datum-found signal, and for thereby generating a control signal to advance the read pointer to skip the first memory location.

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